JITESHRI DASARI

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SUMMARY: Doctoral student with research interest and experience in formal verification of arithmetic circuits.

EDUCATION:

University of Massachusetts (UMass), Amherst – PhD in Electrical and Computer Engineering — Sept 2021 – Present
University of Massachusetts (UMass), Amherst – MS in Electrical and Computer Engineering — May 2018
Symbiosis International University (SIU), Pune, India – B.Tech in Electronics and Telecommunications — May 2016

RELEVANT COURSES:

VLSI Design, Synthesis & Verification of Digital Systems, Computer Architecture, Probability, Hardware Design for Machine Learning Systems, Hardware Verification using Symbolic computation, Microelectronic Fabrication, Embedded Systems, Algorithms

SKILLS:

1. **Programming & HDL:** Verilog, VHDL, SystemVerilog, Python, C/C++, TCL, Perl, MATLAB, TensorFlow, UVM, Java
2. **Design Tools & Softwares:** Synopsys Design Compiler, PrimeTime, Formality, Cadence Virtuoso, Encounter, ncsim, Mentor graphics Modelsim, HSPICE, PSPICE, Multisim, Xilinx ISE, Vivado Design Suite, Eclipse
3. **Academic Tools:** ABC, TDS, Picosat, Singular, Uppaal

WORK EXPERIENCE:

1. **VLSI CAD lab, UMass Amherst,** *Graduate Research Assistant* — **September 2021 – Present**
   - Working on developing novel methods for formal verification of arithmetic circuits under Professor Maciej Ciesielski.
   - Researching existing methods and developing new formal verification tools to achieve better accuracies and speed in large designs.
   - Targeting complex arithmetic circuits and computationally intensive applications.
   - Working on developing formal verification algorithms to target structurally complex architectures.
2. **UMass Amherst,** *Teaching Assistant* — **January 2023 – May 2023**
   - TA for the undergraduate level course on Introduction to Digital and Computer Systems**.** Teaching Verilog and grading assignments and exams.
3. **UMass Amherst,** *Teaching Assistant* — **September 2022 – December 2022**
   - TA for the graduate level course on Neuromorphic Engineering. Helping students with course presentations, projects, and any required software/tools for the projects.
4. **Synopsys Inc., Marlborough, MA,** *R&D Intern* — **May 2022 – August 2022**
   - Worked in the Synopsys Formality R&D team responsible for solving challenging problems in Formal Verification.
   - Contributed significantly to the development of a novel solver useful for formal verification of arithmetic circuits.
   - Used C++ extensively for design and debug.
5. **UMass Amherst,** *Teaching Assistant* — **January 2022 – May 2022**
   - TA for the graduate level course on Embedded Systems. Helping students with questions in assignments and labs and grading the submissions.
6. **Capgemini (Client – Intel), Hudson, MA,** *Senior RTL Engineer* — **July 2020 – June 2021**
   - Worked with a team of Synthesis, Formal verification and PD teams to meet all functional requirements as well as PPA goals.
   - Debugged Caliber violations for Synthesis and Formal Equivalence.
   - Used Synopsys Design Compiler and Cadence Conformal for the required design fixes and RTL changes.
7. **Synopsys Inc., Marlborough, MA,** *Applications Engineer II* — **March 2019 – May 2020**
   - Worked on synthesis, formal equivalence and timing analysis of several customer designs using Design Compiler, Formality and PrimeTime.
   - Resolved several issues related to clock gating, STA, multi-voltage, formal verification, QOR, timing violations etc. using Synopsys tools.
   - Helped CAD engineers in developing custom flows using Synopsys tools.

- Worked with several cross functional teams involving EDA, R&D, CAD, Verification, timing and power, to debug and resolve design and tool issues.

8. Synopsys Inc., Marlborough, MA, *Intern* **October 2018 – March 2019**

- Worked with Applications Engineers to support customers on Design Compiler and PrimeTime issues. Design testcases, research into the issues and formulate different methods to provide solutions to the customers.

9. VLSI CAD lab, UMass Amherst, *Graduate Researcher* **July 2018 – September 2018**

- Contributed to the ongoing research on Formal verification of arithmetic circuits. My work involved running verification experiments, testing the software developed and building technical documentation.

10. UMass Amherst, *Teaching Assistant* **June 2018 – July 2018**

- Assisted students with queries in course which covered the theory of digital circuits and computer systems, Boolean algebra and general techniques for analysis and synthesis of combinational and sequential circuits and grading of homework.

RELEVANT PROJECTS:

1. Implementation of Modified Goldschmidt Division Algorithm, UMass Amherst *Verilog, Modelsim, DC, Encounter, TCL, PrimeTime, SystemVerilog*

- Designed and Implemented the Modified Goldschmidt's Division Algorithm in Verilog and Synthesized the Design using DC.
- Performed functional verification using ModelSim simulations, directed Verilog testbenches and SystemVerilog Immediate Assertions, STA using Synopsys PrimeTime and Physical Implementation using Cadence Encounter in 45nm Standard Cell Technology.

2. Design of an 8-bit Hardware Accelerator (Differential Equation Solver), UMass Amherst *Verilog, Modelsim, DC, Encounter, Formality, TCL, PrimeTime*

- Designed a 2nd order differential accelerator in Verilog and synthesized the design using Synopsys DC.
- Performed Functional verification using Synopsys Formality and Modelsim simulations, STA using PrimeTime and Physical implementation in 45nm standard cell technology using Cadence Encounter. Extracted the block delays and parasitic RC to estimate the actual critical path delay.

3. Implementation of Quine-McCluskey method, independent project *C++, Eclipse IDE*

- Developed a C++ program for the implementation of Quine-McCluskey procedure for logic minimization.
- Used Eclipse IDE for the design and debug of the code.

PUBLICATIONS:

[1] **Dasari, J.** and Ciesielski, M. (2023). Formal Verification of Restoring Dividers made Fast and Simple. *60th Design Automation Conference (DAC), 2023*. (Paper accepted, pending publication)

[2] Ciesielski, M., Yasin, A**.**, & **Dasari, J.** (2022). Functional Verification of Arithmetic Circuits: Survey of Formal Methods. *25th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), 2022, pp. 94-99, doi: 10.1109/DDECS54261.2022.9770161*.